Tuesday 24th May 2022

09:00 - 09:30 (CEST) Opening/Awards

09:30 - 10:30 (CEST) **Keynote Address 1** (Room MAGNA)
Supercomputers and European Sovereignty …
Dr. Mateo Valero Cortés
Director, Barcelona Supercomputing Center, Spain

10:30 - 11:15 (CEST) Coffee Break

11:15 - 12:45 (CEST) **Session 1: Embedded Test and Infrastructure IP** (Room A)
Session Chair: Zebo Peng, Linkoping University, Sweden

11:15 - 11:45 *X-Masking for In-System Deterministic Test* [regular]
Jerzy TYSZER[1], Grzegorz MRUGALSKI[2], Janusz RAJSKI[2], Bartosz WLODARCZAK[1]
[1]Poznan University of Technology, Poland
[2]Siemens Digital Industries Software, Wilsonville, USA

11:45 - 12:15 *Reducing Routing Overhead by Self-Enabling Functional Path Ring Oscillators* [regular]
Tobias KILIAN[1,2], Markus HANEL[1,2], Daniel TILLE[1], Martin HUCH[1], Ulf SCHLICHTMANN[2]
[1]Infineon Technologies, Neubiberg, Germany
[2]Technical University of Munich, Germany

12:15 - 12:45 *Research on Path Delay with BTI Recovery Effect* [case-study]
Jiebing WU, Yongsheng SUN, Yukai LIN, Yuan WANG, Mingna FAN, Junlin HUANG
Hisilicon Technologies Co. Ltd, Shenzhen, China

11:15 - 12:45 (CEST) **Session 2: Security and Trust** (Room MAGNA)
Session Chair: Haralampos Stratigopoulos, Sorbonne University/LIP6, France

11:15 - 11:45 *Evaluating Security of New Locking SIB-based Architectures* [regular]
Yogendra SAO[1], Anjum RIAZ[2], Satyadev AHLAWAT[2], Sk. Subidh ALI[1]
[1]Indian Institute of Technology Bhilai, India
[2]Indian Institute of Technology Jammu, India

11:45 - 12:15 *TaintLock: Preventing IP Theft through Lightweight Dynamic Scan Encryption using Taint bits* [regular]
Jonti TALUKDAR, Arjun CHAUDHURI, Krishnendu CHAKRABARTY
Duke University, USA

12:15 - 12:45 *A Lightweight, Plug-and-Play and Autonomous JTAG Authentication IP for Secure Device Testing* [case-study]
Sebastien LAPEYRE[1], Nicolas VALETTE[1], Marc MERANDAT[1], Marie-Lise FLOTTES[2], Bruno ROUZEYRE[2], Arnaud VIRAZEL[2],
[1]INVIA, Meyreuil, France
[2]University of Montpellier/CNRS/LIRMM, France

11:15 - 12:45 (CEST) **Vendor Session 1** (Room B)
Session Chair: Stephan Eggersgluess, Siemens EDA, Germany

11:15 - 11:45 *Improving Test Quality and Reliability via In-system/In-field Testing*
Lee HARRISON
SIEMENS EDA, United Kingdom

11:45 - 12:15 *How ACS enables an Open Innovation Ecosystem for AI/ML applications in the Semiconductor Value Chain*

Matthias SAUER, Sonny BANWARI
ADVANTEST, Boeblingen, Germany

12:15 - 12:45 The Need for New DFT Approaches to Scan
Thomas KOEHLER
TERADYNE, Munich, Germany

12:45 - 14:00 (CEST) Lunch

14:00 - 15:00 **Session 3: Functional Safety** (Room A)
Session Chair: Paolo Bernardi, Politecnico di Torino, Italy

14:00 - 14:30 *A Data-driven Approach for Fault Detection in the Alternator Unit of Automotive Systems* [case-study]
Mehdi TAHOORI[1], Arunkumar VIJAYAN[1], Ewald KINTZLI[2], Timm LOHMANN[2], Juergen Hans HANDL[2]
[1]Karlsruhe Institute of Technology, Germany
[2]SEG Automotive, Stuttgart, Germany

14:30 - 15:00 *On Extracting Reliability Information from Speed Binning* [hot-topic]
Zahra NAJAFI HAGHI, Florian KLEMME, Hussam AMROUCH, Hans-Joachim WUNDERLICH
University of Stuttgart, Germany

14:00 - 15:00 (CEST) **Embedded Tutorial Session 1** (Room MAGNA)
IEEE P2427 - Analog defect Simulation in the industry of tomorrow
Organizer: Anthony COYETTE (Onsemi, Belgium)

14:00 - 14:20 *A General Introduction: Scope, Purpose and Status*
Anthony COYETTE
Onsemi, Belgium

14:20 - 14:40 *Defect Classification and Defect Coverage Reporting*
Jo GUNNES
NXP, The Netherlands

14:40 - 15:00 *Analog Defect Simulation Applications on Digital and Alternate Tests*
Devanathan VARADARAJAN
Texas Instruments, USA

14:00 - 15:00 (CEST) **Poster Session 1** (5 minutes per paper) (Room B)
Session Chair:

A Generic Fast and Low Cost BIST Solution for CMOS Image Sensors
Julia LEFEVRE[1,2], Philippe DEBAUD[2], Patrick GIRARD[2], ARNAUD VIRAZEL[2]
[1]STMicroelectronics, Grenoble, France
[2]University of Montpellier/CNRS/LIRMM, France

FPGA Design Deobfuscation by Iterative LUT Modifications at Bitstream Level
Michail MORAITIS, Elena DUBROVA
Royal Institute of Technology, Stockholm, Sweden

Quality Assessment of RFET-based Logic Locking Protection Mechanisms using Formal Methods
Marcel MERTEN, Sebastian HUHN, Rolf DRECHSLER
University of Bremen, Germany

RRAM Crossbar-Based Fault-Tolerant Binary Neural Networks (BNNs)
Anteneh GEBREGIORGIS, Artemis ZOGRAFOU, Said HAMDIOUI
Delft University of Technology, The Netherlands

Detection of Malicious FPGA Bitstreams using CNN-Based Learning
Jayeeta CHAUDHURI, Krishnendu CHAKRABARTY
Duke University, USA

Hierarchical Memory Diagnosis
Guilherme CARDOSO MEDEIROS[1], Moritz FIEBACK[1], Anteneh GEBREGIORGIS[1], Mottaqiallah TAOUIL[1], Leticia Bolzani POEHLS[2], Said HAMDIOUI[1]
[1]Delft University of Technology, The Netherlands
[2]IDS, RWTH Aachen, Germany

Novel Design For Test (DFT) Concept to Check the Spectral Mask Compliance Defined in the IEEE Std. 802.15.6-2012 of Wireless-Body-Area-Network (WBAN) IC-Devices
Alexander OLESZCZUK[1,2], Mohamed THOUABTIA[1], Martin ALLINGER[1], Jurgen Rober[1], Robert Weigel[2]
[1]eesy-IC GmbH, Erlangen, Germany
[2]Friedrich-Alexander University, Erlangen, Germany

Graph Theory Approach for Multi-site ATE Board Parameter Extraction
Abraham STEENHOEK[1], Praise FARAYOLA[1], Isaac BRUCE[1], Shravan CHAGANTI[2], Abalhassan SHEIKH[2], Srivaths RAVI[2], Degang CHEN
[1]Iowa State University, Ames, USA
[2]Texas Instruments, USA

Prediction of Thermally Accelerated Aging Process at 28 nm
Parvez CHANAWALA, Ian HILL, Seyed Arash SHEIKHOLESLAM (UBC), Andre IVANOV
University of British Columbia, Vancouver, Canada

15:00 - 16:00 (CEST) Coffee Break & **Poster Session 1**

16:00 - 17:30 (CEST) **Session 4: Safety of Circuits and Systems** (Room A)
Session Chair:

16:00 - 16:30 *Machine learning based soft error rate estimation of pass transistor logic in high-speed communication* [case-study]
Zhe ZHANG[1], Jan LAPPAS[2], Andre CHINAZZO[2], Christian WEIS[2], Zhihang WU[3], Leibin NI[3], Mehdi TAHOORI[1], Norbert WEHN[2]
[1]Karlsruhe Institute of Technology, Germany
[2]Technical University Kaiserslautern, Germany
[3]Huawei Technologies Co. Ltd., Shenzhen, China

16:30 - 17:00 *Super Acceleration of Dilithium in MPSoC Critical Environments* [case-study]
Johanna SEPULVEDA[1,2], Dominik WINKLER[2]
[1]Airbus Defence and Space, Germany
[2]Technical University Munich, Germany

17:00 - 17:30 *Real-Time Control-Flow Integrity for Multicore Mixed-Criticality IoT Systems* [hot-topic]
Vahid EFTEKHARI, Paolo PRINETTO, Gianluca ROASCIO
Politecnico di Torino, Italy

16:00 - 17:30 (CEST) **Special Session 1** (Room MAGNA)
RF 5G Test
Organizer: William EISENSTADT (Univ. Florida, USA)

16:00 - 16:30 *Addressing the Challenges of 5G Production Test*
Mark Roos, CEO and Devin Morris, Senior RF Applications Engineer
Roos Instruments, Inc., Santa Clara, USA

16:30 - 17:00 *RF and mmW test activities at CEA-Leti*
José Luis González-Jiménez and Christopher MOUNET
UGA/CEA-Leti, Grenoble, France

17:00 - 17:15 *Feature selection techniques for indirect test and statistical calibration of mm-wave integrated circuits*
Manuel J. Barragan[1], Gildas Leger[2], Florent Cilici[3], Estelle Lauga-Larroze[1], Salvador Mir[1], Sylvain Bourdel[1]
[1]UGA/G-INP/CNRS/TIMA, Grenoble, France
[2]IMSE-CNM, CSIC, Universidad de Sevilla, Sevilla, Spain
[3]NXP, Toulouse, France

17:15 - 17:30 *Integrated Characterization Solutions for ICs and Devices Beyond 100 GHz*
M. Margalef-Rovira[1], I. Alaji1, H. Ghanem[1], G. Ducournau[1], and C. Gaquiere[2]
[1]Univ. Lille, CNRS, Centrale Lille, Yncrea Lille, Univ. Polytechnique Hauts-de-France, Lille, France
[2]MC2-Technologies, 59493 Villeneuve-d'Ascq, France

16:00 - 17:30 (CEST) **Industry Case-Study Presentations Session 1** (Room B)
Session Chair: Wim Dobbelaere, ON Semiconductor, Belgium
Session Co-Chair: Davide Appello, STMicroelectronics, Italy

16:00 - 16:20 *Strategies for Enabling Quantum Development with Test and Measurement at millikelvin range focussing on pre-characterization*
Jack DEGRAVE[1], Philip KRANTZ[2], Dong-Thuc KNOBBE[1]
[1]FormFactor, USA
[2]Keysight, USA

16:20 - 16:40 *Challenges and Solutions for Automotive Cold Test Elimination*
Chen HE
NXP Semiconductors, USA

16:40 - 17:00 *RETE: DfRT, Test for Reliability & Data Analysis for zero defects and zero scraps*
Mauro PIPPONZI, Alessandro MASERI, Luca MORICONI
ELES Semiconductor Equipment, Italy

17:00 - 17:20 *3D interconnect Test Challenge*
Sreejit CHAKRAVARTY
Intel, USA

17:30 - 19:00 (CEST) **Panel Session 1 (with wine & cheese)** (Room MAGNA)
I wish IJTAG would do this ...
Organizer: Michele PORTOLAN (Grenoble-INP, France), Jeff REARICK (AMD, USA)
Moderator: Jeff REARICK (AMD, USA)
Participants:
Jean-Francois COTE (Siemens EDA,USA),
Martin KEIM (Siemens EDA, USA) (note taker for IEEE 1687 WG)
Two active users IEEE 1687 (TBD)
Michele PORTOLAN (Grenoble-INP/TIMA, France)

Wednesday 25th May 2022

08:30 - 09:30 (CEST) **Keynote Address 2** (Room MAGNA)

AI-Assisted Yield Learning
Dr. Yu Huang
EDA Chief Architect, HiSilicon Technologies Co. Ltd, China

09:30 - 10:30 (CEST) **Poster Session 2** (5 minutes per paper)
Session Chair:

Trojan Insertions of Fully Programmable Valve Arrays
Nadun SINHABAHU[1], Jian-De LI[2], Katherine Shu-Min LI[1], Syng-Jyan WANG[2], Tsung-Yi HO[3]
[1]National Sun Yat-Sen University, Taiwan
[2]National Chung-Hsing University, Taiwan
[3]National Tsing Hua University, Taiwan

Smart Redundancy Schemes for ANNs against Fault Attacks
Troya KöYLü, Said HAMDIOUI, Mottaqiallah TAOUIL
Delft University of Technology, The Netherlands

A Novel Collaborative SSD Test Case Clustering Method Associating I/O Workload and Function Coverage
Gyohun JEONG, Sangmin KIM, Hyelyun KIM, Sunghee LEE
Samsung Electronics, Hwaseong, Republic of Korea

Novel Method to Measure Common Mode Transient Immunity of Isolators
Mohamed THOUABTIA, Alexander OLESZCZUK, Thomas GIRG, Martin ALLINGER
eesy-IC GmbH, Erlangen, Germany

On-Chip training of Crosstalk Predictors to Fit Uncertainties
Rezgar SADEGHI, Ehsan AKBARI, Mohamad Ali SABER
University of Tehran, Iran

On-Line Reliability Estimation of Ring Oscillator PUFs
Sergio VINAGRERO GUTIERREZ, Giorgio DI NATALE, Elena Ioana VATAJELU
UGA/CNRS/G-INP/TIMA, Grenoble, France

Concurrent Error Detection for LSTM Accelerators
Nooshin NOSRATI, Seyedeh Maryam GHASEMI, Mahboobe SADEGHIPOUR ROODSARI, Zainalabedin NAVABI
University of Tehran, Iran

Process and Runtime Variation Robustness for Spintronic-Based Neuromorphic Fabric
Soyed Tuhin AHMED, Hefenbrock MICHAEL, Mahta MAYAHINIA, Christopher MÜNCH, Mehdi TAHOORI
Karlsruhe Institute of Technology, Germany

Effective techniques for automatically improving the transition delay fault coverage of Self-Test Libraries
Sandro SARTONI[1], Riccardo CANTORO[1], Francesco GARAU[1], Patrick GIRARD[2], Nima KOLAHIMAHMOUDI[1], Matteo SONZA REORDA[1], ARNAUD VIRAZEL[2]
[1] Politecnico di Torino, Italy
[2]University of Montpellier/CNRS/LIRMM, France

09:30 - 10:30 (CEST) **Special Session 2** (Room MAGNA)

Test, Reliability and Functional Safety trends for Automotive System-on-Chip
Organizer: Paolo Bernardi, Politecnico di Torino (Italy)

09:30 - 09:50 *Self-mitigation properties on Image segmentation Neural Networks*
R. Mariani, A. Ruospo, G. Gavarini, C. De Sio, L. Sterpone, M. Sonza, J. Aribido, E. Sanchez
Nvidia (USA), Politecnico di Torino (Italy)

09:50 - 10:10 *A Machine Learning Framework to catch Inter-Wafer Process Variations in Microcontrollers Performance Prediction*
M. Huch, N. Bellarmino, R. Cantoro, Tobias Kilian, R. Martone, U. Schlichtmann, G. Squillero
Infineon Technologies (Germany), Politecnico di Torino (Italy)

10:10 - 10:30 *A System-level Test and Burn-In oriented Test Equipment*
D. Appello, F. Angione, P.Bernardi, T. Foscale, V. Tancorre, R. Ugioli
STMicroelectronics (Italy), Politecnico di Torino (Italy)

09:30 - 10:30 (CEST) **Industry Case-Study Presentations Session 2** (Room C)
Session Chair: Davide Appello, STMicroelectronics, Italy
Session Co-Chair: Wim Dobbelaere, ON Semiconductor, Belgium

09:30 - 09:50 *Evaluating Burn-In related Metrics for large Automotive Systems-on-Chip*
Francesco ANGIONE[1], Paolo BERNARDI[1], Andrea CALABRESE[1], Stefano QUER[1], Davide APPELLO[2], Vincenzo TANCORRE[2], Roberto UGIOLI[2]
[1] Politecnico di Torino, Italy
[2] STMicroelectronics, Italy

09:50 - 10:10 *MBSA Approaches Applied to Next Decade Digital Components*
Tiziano FIORUCCI[1], Jean-Marc DAVEAU[1], Emmanuel ARBARETIER[2], Giorgio DI NATALE[3], Philippe ROCHE[1], Thomas JACQUET[2]
[1]STMicroelectronics, Crolles, France
[2]APSYS-AIRBUS, France
[3]Univ. Grenoble Alpes/CNRS/TIMA, France

10:10 - 10:30 *Monitoring and controlling handler temperature*
Guy DECABOOTER
Onsemi, Belgium

10:30 - 11:15 (CEST) Coffee Break & **Poster Session 2**

11:15 - 12:45 (CEST) **Panel Session 2** (Room MAGNA)
Can DPPM of AMS circuits be accurately estimated from their defect coverage?
Organizer/Moderator: Vladimir ZIVKOVIC (Infineon Technologies, Denmark)
Participants:
Mayukh BHATTACHARYA (Synopsys, USA),
Dieter DRAXELMAYR (Infineon Technologies, Austria),
Bram KRUSEMAN (NXP Semiconductors, The Netherlands),
Stephen SUNTER (Siemens EDA, Canada),
Haralampos STRATIGOPOULOS (Sorbonne University/LIP6, France)

12:45 - 14:00 (CEST) Lunch

14:00 - 15:00 (CEST) **Session 5: Validation and verification** (Room A)
Session Chair: Virendra Singh, Indian Institute of Technology, Bombay

14:00 - 14:30 *Enabling Coverage-Based Verification in Chisel* [regular]
Andrew DOBIS, Hans Jakob DAMSGAARD, Enrico TOLOTTO, Kasper HESSE, Tjark PETERSEN, Martin SCHOEBERL
Technical University of Denmark, Lyngby, Denmark

14:30 - 15:00 *SpinalFuzz: Coverage-Guided Fuzzing for SpinalHDL Designs* [case-study]

Katharina RUEP, Daniel GROSSE
Johannes Kepler University, Linz, Austria

14:00 - 15:00 (CEST) **Embedded Tutorial Session 2** (Room B)
Power Aware Test
Organizer: Likith Kumar MANCHUKONDA, Synopsys Inc., USA

14:00 - 14:20 *Memory and Scan Test Implementation*
Likith Kumar MANCHUKONDA
Synopsys Inc., USA

14:20 - 14:40 *Scan Synthesis, Placement and Routing*
Karthikeyan NATARAJAN
Synopsys Inc, USA

14:40 - 15:00 *Automatic Pattern Generation*
Manish ARORA
Synopsys Inc, USA

14:00 - 15:00 (CEST) **PhD Forum Session** (3 minutes per paper) (Room C)
Session Chair: Ernesto Sánchez, Politecnico di Torino, Italy
Session Co-chair: Liviu Miclea, Technical University of Cluj-Napoca, Romania

A Pipelined AUTOSAR Communication ASIP
Ahmed HAMED[1,2], Watheq EL-KHARASHI[1,3], Ashraf SALEM[1,2], Mona SAFAR[1]
[1]Ain Shams University, Cairo, Egypt
[2]Siemens Digital Industries Software, Cairo, Egypt
[3]University of Victoria, Canada

A Platform for Structural Analysis of Logic Locking Using Machine Learning
Prabuddha CHAKRABORTY[1], Jonathan CRUZ[1], Abdulrahman ALAQL[1,2], Swarup BHUNIA[1]
[1]University of Florida, USA
[2]KACST, Saudi Arabia

Analysis and Simulation of Logic-In-Memory Operations
Pietro INGLESE, Elena Ioana VATAJEL, Giorgio DI NATALE (UGA/CNRS/G-INP/TIMA, Grenoble, France)

Control Flow Error Detection Techniques Assessment for Embedded Software Development and Validation
Mohammadreza AMEL SOLOUKI, Jacopo SINI, Massimo VIOLANTE (Politecnico di Torino, Italy)

Defect Analysis of a Spintronic Synapse for Spiking Neural Networks
Salah DADDINOUNOU, Elena Ioana VATAJELU (UGA/CNRS/G-INP/TIMA, Grenoble, France)

DNN Hardware Reliability Assessment and Enhancement
Mahdi TAHERI, Maksim JENIHHIN, Masoud DANESHTALAB (Tallin University of Technology, Estonia)

Embedded memory testing: from power measurements to defect analysis
Giorgio INSINGA, Paolo BERNARDI, Riccardo CANTORO (Politecnico di Torino, Italy)

Improving the Design for Testability of Integrated Circuits Using Formal Methods and AI Techniques
Payam HABIBY (University of Bremen, Germany)

Manufacturing Testing and Functional Safety techniques for Automotive SoCs
Francesco ANGIONE, Paolo BERNARDI, Riccardo CANTORO (Politecnico di Torino, Italy)

Memristor-based Security Primitives
Sergio VINAGRERO GUTIERREZ, Elena Ioana VATAJELU, Giorgio DI NATALE (UGA/CNRS/G-INP/TIMA, Grenoble, France)

New Solutions for Generating Functional Sequences Maximizing the Sustained Switching Activity of Complex SoCs
Nikolaos DELIGIANNIS (Politecnico di Torino)

New techniques to detect and mitigate aging effects in advanced semiconductor technologies
Sandro SARTONI (Politecnico di Torino, Italy)

Qualification methodology for ISO26262 certification of automotive SoC systems
Tiziano FIORUCCI[1,2], Giorgio DI NATALE[2]
[1]STMicroelectronics
[2]UGA/CNRS/G-INP/TIMA, Grenoble, France

Reliability Assessment of Neural Networks in GPUs
Juan GUERRERO (Politecnico di Torino, Italy)

Resiliency to Soft-Errors for Embedded Processors Using ML-based Checkers
Nooshin NOSRATI[1], Zainalabedin NAVABI[1], Maksim JENIHHIN[2]
[1]University of Tehran, Iran
[2]Tallin University of Technology, Estonia

Strategies and Evaluation Methods to reach Ultra-Reliability in Automotive Systems-on-Chip
Giusy IARIA, Paolo BERNARDI (Politecnico Di Torino, Italy)

Tools for the Analysis of Simulation Dumps and the Evaluation of Burn-in Techniques
Andrea CALABRESE, Giovanni SQUILLERO, Stefano QUER (Politecnico di Torino, Italy)

Using ML for Back-Annotating Low-Level Effects in a System-Level Framework
Katayoon BASHARKHAH, Zainalabedin NAVABI (University of Tehran, Iran)

15:00 - 16:00 (CEST) **Keynote Address 3** (Room MAGNA)
DFX: Exploring the Design Space for Quality
Kaushik Narayanun
Vice-president Engineering, NVIDIA, USA

16:00 - 17:00 (CEST) Coffee Break & PhD Forum Posters

17:00 - 22:00 Social Event & Gala dinner

Thursday 26th May 2022

08:30 - 09:30 (CEST) **Keynote Address 4** (Room MAGNA)

SiGe BiCMOS Technology with Advanced Integration Solutions for mm-Wave and THz Applications

Dr.-Ing. Mehmet Kaynak
Leibniz Institute for High Performance Microelectronics (IHP), Germany

09:30 - 10:30 (CEST) **Session 6: Analog/Mixed-Signal and RF Test** (Room A)
Session Chair: Jordi Madrenas, UPC, Barcelona, Spain

9:30 - 10:00 *WLAN Rx PER Test Implementation in ATE* [case-study]
Alban Haynse IMMANUEL, Jey NITHYANANDAM
Infineon Technologies, Bangalore, India

10:00 - 10:30 *AMS Test Vector Generation using AMS Verification and IEEE P1687.2* [hot-topic]
Vladimir ZIVKOVIC[1], Mogens ISAGER[1], Michele PALAZZI[2], Ming Chuen Alvan LAM[2]
[1]Infineon Technologies, Denmark
[2]Infineon Technologies, USA

09:30 - 10:30 (CEST) **Special Session 3** (Room MAGNA)
Impact of Atmospheric and Space Radiation on Sensitive Electronic Devices
Organizer: Luigi DILILLO (University of Montpellier, CNRS, LIRMM, FRANCE)

9:30 - 9:50 *Radiative environments and prediction tools*
Frédéric Wrobel
IES, University of Montpellier, France

9:50 - 10:10 *Effects of radiation on electronic memories*
Lucas Matana Luza
LIRMM, University of Montpellier, CNRS, France

10:10 - 10:30 *Effects of radiation on microprocessors*
Luis Entrena
University Carlos III, Madrid, Spain

09:30 - 10:30 (CEST) **McCluskey PhD Contest Session** (Room B)
Session Chair: Alberto Bosio, Lyon Institute of Nanotechnology, France
Session Co-chair: Alessandro Savino, Politecnico di Torino, Italy

09:30 - 09:50 *New Techniques for On-line Testing and Fault Mitigation in GPUs*
Josie RODRIGUEZ CONDIA
Politecnico di Torino, Italy

09:50 - 10:10 *Next Generation Design For Testability, Debug and Reliability Using Formal Techniques*
Sebastian HUHN
University of Bremen, Germany

10:10 - 10:30 *On Design for Reliability for Digital VLSI Systems*
Chih-Hao WANG
National Sun Yat-sen University, Taiwan

10:30 - 11:15 (CEST) Coffee Break & **Posters McCluskey PhD Contest**

11:15 - 12:45 (CEST) **Session 7: Diagnosis and Stress Test** (Room A)
Session Chair:

11:15 - 11:45 *CNN-based Data-Model Co-Design for Efficient Test-termination Prediction* [regular]
Hongfei WANG, Zhanfei WU, Wei LIU
Huazhong University of Science and Technology, China

11:45 - 12:15 *Optimized diagnostic strategy for embedded memories of Automotive Systems-on-Chip* [regular]
Paolo BERNARDI[1], Giorgio INSINGA[1], Giovanni PAGANINI[1], Riccardo CANTORO[1], Peter BEER[2], Nellina MAUTONE[2], Pierre SCARAMUZZA[2], Giambattista CARNEVALE[2], Matteo COPPETTA[2], Rudolf ULLMANN[2]
[1]Politecnico Di Torino, Italy
[2]Infineon Technologies, Germany and Italy

12:15 - 12:45 *An Optimized Burn-In Stress Flow targeting Interconnections logic to Embedded Memories in Automotive Systems-on-Chip* [regular]
Francesco ANGIONE[1], Paolo BERNARDI[1], Gabriele FILIPPONI[1], Matteo SONZA REORDA[1], Davide APPELLO[2], Vincenzo TANCORRE[2], Roberto UGIOLI[2]
[1]Politecnico Di Torino, Italy
[2]STMicroelectronics, Agrate Brianza, Italy

11:15 - 12:45 (CEST) **Special Session 4** (Room MAGNA)
Machine Learning for Test, Diagnosis, Post-Silicon Validation and Yield Optimization
Organizer: Ilia Polian (Univ. Stuttgart, Germany), Matteo Sonza Reorda (Politecnico di Torino, Italy)

11:15 - 11:45 *Learning to Tune in Post-silicon Validation*
Dirk Pflüger
University of Stuttgart, Germany

11:45 - 12:15 *Adapting Machine Learning to Test and Diagnosis Problems*
Krishnendu Chakrabarty
Duke University, Durham, NC, USA

12:15 - 12:30 *Brain-Inspired Machine Learning for Semiconductor Test and Reliability*
Hussam Amrouch
University of Stuttgart, Germany

12:30 - 12:45 *Industrial Solutions for Machine-Learning-Enabled Yield Optimization and Test*
Matthias Sauer
Advantest Europe, Boeblingen, Germany

11:15 - 12:45 (CEST) **Vendor Session 2** (Room B)
Session Chair: Stephan Eggersgluess, Siemens EDA, Germany

11:15 - 11:45 Machine Learning for DFT and ATPG
Yu HUANG
HiSILICON Inc., Shenzen, China

11:45 - 12:15 Functional Safety Challenges and Solutions for the ARM® MaliTM-G78AE GPU
Prashant KULKARNI
ARM, United Kingdom

12:15 - 12:45 *3D IC DFT Implementation and Interconnect Test Based on IEEE 1838*
Vivek CHICKERMANE[1], Sagar KUMAR[1], Rajesh KHURANA[1], Lukasz KOTYNIA, Frederic AZOULAU
[1]CADENCE Design Systems, USA
[2]CADENCE Design Systems, POLAND

12:45 - 14:00 (CEST) Lunch

14:00 - 15:00 (CEST) **Session 8: Emerging Technologies Test** (Room A)

Session Chair : Ioana Vatajelu, UGA/CNRS/G-INP/TIMA, Grenoble, France
14:00 - 14:30 *On the Impact of Hardware Timing Errors on Stochastic Computing based Neural Networks* [regular]
Florian NEUGEBAUER[1], Stefan HOLST[2], Ilia POLIAN[1]
[1]University of Stuttgart, Germany
[2]Kyushu Institute of Technology, Iizuka, Japan

14:30 - 15:00 *PVT Analysis for RRAM and STT-MRAM-based Logic Computation-in-Memory* [regular]
Moritz FIEBACK[1], Christopher MÜNCH[2], Anteneh GEBREGIORGIS[1], Guilherme CARDOSO MEDEIROS[1], Mottaqiallah TAOUIL[1], Said HAMDIOUI[1], Mehdi TAHOORI[2]
[1]Delft University of Technology, The Netherlands
[2]Karlsruhe Institute of Technology, Germany

14:00 - 15:00 (CEST) **Embedded Tutorial Session 3** (Room MAGNA)
Post-Silicon SoC (System on Chip) Validation Coverage Challenges
Organizer: Chinna PRUDVI (Intel Corporation, USA)

Speakers: Chinna PRUDVI (Intel, USA), SANKARAN MENON (Intel, USA), Rathish JAYABHARATHI (Intel, USA), Bhvanesh MATHUR (Intel USA), Spencer MILLICAN (Auburn University, USA)

14:00 - 14:15 *Introduction – Coverage for Manufacturing and Validation*
14:15 - 14:30 *Pre-to-Post Silicon Validation Coverage*
14:30 - 14:45 *Post-Silicon SOC Validation Coverage Challenges*
14:45 - 15:00 *Conclusions and future work: AI and machine-learning opportunities*

14:00 - 15:00 (CEST) **Vendor Session 3** (Room B)
Session Chair: Stephan Eggersgluess, Siemens EDA, Germany

14:00 - 14:30 Rich Interactive Test Database (RITdB): The Interplanetary Database for Manufacturing
Mark ROOS
ROOS Instruments Inc., Santa Clara, USA

14:30 - 15:00 Testing and Analyzing Throughout the Silicon Lifecycle
Robert RUIZ, Ramsay ALLEN
SYNOPSYS Inc., Mountain View, USA

15:00 - 15:30 (CEST) **Awards & Closing** (Room MAGNA)